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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,237	01/10/2006	Martin J. Edward	GB03 0112 US1	6993

24738 7590 07/20/2009

PHILIPS INTELLECTUAL PROPERTY & STANDARDS
PO BOX 3001
BRIARCLIFF MANOR, NY 10510-8001

EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
07/20/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/564,237	EDWARD, MARTIN J.	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/03/2009*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sato et al (5,712,652) hereinafter, Sato in view of Aoki et al (6,307,532) hereinafter Aoki.

4. In regards claim 1, Sato teaches an active matrix array comprising (col. 1, lines 19-20):

an array of matrix elements arranged in rows and columns, each matrix element comprising a circuit (fig. 1 pixels circuits (13));

a plurality of first and second column conductors, each arranged for inputting data signals to or outputting data signals from the matrix elements of a respective column in first time periods (fig. 1 (1-1a and 1-1b) and col. 7 data driver signal); and

wherein the first column conductors supply first voltage and the second column conductors supply second voltage to each matrix element and wherein the first voltage and the second voltage are separate voltages (fig. 1 (1-1 and 2-2) col. 9, lines 27-67)).

Sato fails to expressly teach providing power supply voltages for the circuit to the matrix element in second time periods interspersed between the first time periods.

However, Aokia teaches providing power supply voltages for the circuit to the matrix element in second time periods interspersed between the first time periods (fig. 5 pixel data and precharge signal col. 10, lines 6-45)).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Sato to include the use of providing power supply voltages for the circuit to the matrix element in second time periods interspersed between the first time periods as taught by Aokia in order to preventing deterioration of image quality owning to delay of the signal transporting speed as stated in abstract (abstract of Aoki).

5. In regards to claim 12, Sato teaches a method of operating an active matrix array device (col. 1, lines 19-20) comprising a plurality of first and second column conductors (fig. 1 1-1a, 1-2,a, 1-1b, and 1-2b) and an array of matrix elements arranged in rows and columns (fig. 1 1-1, and 2-1), wherein each matrix element comprises a circuit

requiring power supply voltages to be supplied to the circuit(col. 9, lines 22-60), the method comprising:

connecting each matrix element to one first and one second column conductors (fig. 13, 1-1 and 1-1b);

in first time periods, inputting a data signal to or outputting a data signal from the matrix element via the first column conductor (col. 9, lines 20-60 fig. 7 data driver signal) and

wherein the first column conductors supply first voltage and the second column conductors supply second voltage to each matrix element (col. 9, lines 25-35)

Sato fails to expressly teach providing in second time periods interspersed with the first time periods, providing the power supply voltages to the matrix element via the first and second column conductors.

However, Aokia teaches providing in second time periods interspersed with the first time periods, providing the power supply voltages to the matrix element via the first and second column conductors (fig. 5 pixel data and precharge signal col. 10, lines 6-45)).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Sato to include the use of providing in second time periods interspersed with the first time periods, providing the power supply voltages to the matrix element via the first and second column conductors as taught by Aokia in order to preventing deterioration of image quality owning to delay of the signal transporting speed as stated in abstract (abstract of Aoki).

6. In regards to claim 2, Sato modified by Aokia teaches the active matrix array according to claim 1, wherein each matrix element further comprises differentiating means for operating according to whether the column conductors are being supplied with the power supply voltages or whether the column conductors are being supplied with the data signals (fig. 3 (114) of Aokia).

7. In regards to claim 3, Sato as modified by Aokia teaches the active matrix array according to claim 2, further comprising:

a plurality of row conductors, each arranged for inputting a control signal to the matrix elements, the control signal being such as to indicate to the matrix elements when the column conductors are being supplied with the power supply voltages and when the column conductors are being supplied with the data signals

wherein the differentiating means in each matrix element operates in response to the control signal (col. 11, lines 24-54 Aokia).

8. In regards to claim 4, Sato as modified by Aokia teaches the active matrix array according to any of claim 1, wherein the matrix elements are pixels for a display each pixel comprises, a pixel electrode and a pixel select switching means coupled to the pixel electrode (col. 9, lines 20-60 Sato).

9. In regards to claim 5, Sato as modified by Aokia teaches the active matrix array according to claim 4, wherein the circuit is a refresh circuit for refreshing the pixel electrode (col. 9, lines 28-65 Sato).

10. In regards to claim 6, Sato as modified by Aokia teaches the active matrix array according to claim 4, wherein the pixels are adapted such that the control signal is used to indicate to the pixel when the column conductors are carrying the power supply voltages and to switch the pixel from a state where the pixel electrode receives picture data from the column conductors to a state where the pixel electrode receives inverted refresh picture data from the circuit (col. 3, (172 and 106) and col. 11, lines 24-54 Aokia).

11. In regards to claim 7, Sato as modified by Aokia teaches the active matrix array according to any of claim 1, wherein the circuit comprises a CMOS inverter (col. 9, lines 28-65 Sato CMOS inverters Sato).

12. In regards to claim 8, Sato as modified by Aokia teaches the active matrix array of any of claim 4, wherein each matrix element further comprises a first control thin film transistor, (TFT) having a gate terminal coupled to one of the row conductors arranged to allow picture data to be provided to the pixel electrode only when the control signal is set such as to turn the first control TFT on (fig. 1 (6) col. 11, lines 42-67 Sato).

13. In regards to claim 9, Sato as modified by Aokia teaches the active matrix array according to claim 8, wherein each matrix element further comprises a second control TFT having a gate terminal coupled to one of the row conductors arranged to allow refresh data to be provided the pixel electrode only when the control signal is set such as to turn the second control TFT on and the first control TFT off (fig. 1 (7) col. 11, lines 42-67 Sato).

14. In regards to claim 10, Sato as modified by Aokia teaches the active matrix array according to claim 9, wherein each matrix element further comprises a third control TFT having (fig. 10 (27) Sato) a gate terminal coupled to one of the row conductors arranged to allow the power supply voltages to be supplied to the circuit only when the control signal is set such as to turn the second and third control TFTs on and the first control TFT off (fig. 10 (27) col. 15-16, lines 45-18 Sato).

15. In regards to claim 11, Sato as modified by Aokia teaches the active matrix array according to any of claim 1, wherein each matrix element is coupled to first and second adjacent column conductors (fig. 1 (1-1a and 1-1b) Sato);

a first power supply voltage level is supplied to the circuits of a first column of matrix elements via the first column conductor arranged to also input or output data signals to or from the first column of matrix elements ((fig. 3 PV1 Aokia)), and

a second power supply voltage level is supplied to the circuits of the first column of matrix elements via the second column conductor arranged to also input or output data signals to or from a second column of matrix elements ((fig. 3 PV2 Aokia)).

Response to Arguments

16. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Grant D Sitta/
Examiner, Art Unit 2629
July 9, 2009